



# Tiny Light Engine for Large Scale LED Lighting

## Message from the Coordinator

The first 24 months of the project have passed and the project partners can look back at very active twenty-four months with a lot of ups and downs. All project partners are committed to the project and the cooperation within the consortium is good and fruitful.

There have been some challenges in the past and there will for sure be some in the future, but the consortium looks full of energy and zest for action into the last year of the project and is confident to reach the project goals.

### Newsletter / November 2018 - Issue 4

#### Consortium

7 partners (4 countries)

Project number: **731466**

Project website: [www.ledlum-project.eu](http://www.ledlum-project.eu)

#### Project Coordinator

Dr. Klaus-Michael KOCH

[coordination@ledlum-project.eu](mailto:coordination@ledlum-project.eu)

Project start: **1<sup>st</sup> November, 2016**

Duration: **3 years**

#### Technical Leader

Mickey Madsen

[mickey@nopoc.com](mailto:mickey@nopoc.com)

Total cost: **EUR 4,118.521,25**

EC contribution: **EUR 4,118.821,25**

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PHOTONICS PUBLIC PRIVATE PARTNERSHIP

The LEDLUM project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 731466. This project is an initiative of the Photonics Public Private Partnership.

# Technical and Review Meeting in Lyngby

*From 10<sup>th</sup> to 12<sup>th</sup> of October the LEDLUM partners met for a Technical as well as a Review Meeting in Lyngby, Denmark, hosted by partner Technical University of Denmark (DTU).*

On the first day all partners presented and reflected on their individual completed work. Then the consortium was split into two groups to focus on and discuss the interaction between the partners in the past. The findings of this group discussion have then been used to take the lessons learned and to define the hot topics for the next day.

On the second day the consortium split into two groups again. One group participated at the Review meeting and the second group continued with the technical meeting further worked on the hot topics. To provide an in-depth update of the progress of the action and to assess the degree to which the work plan has been carried out was the main purpose of the review meeting.

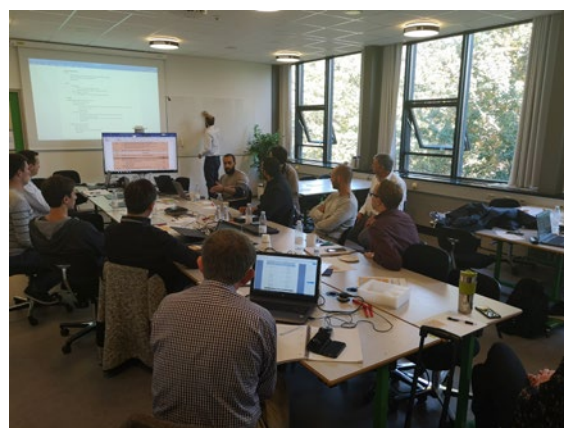
The partners presented the work that was performed during the first 18 project months in each work package and highlighted the major achievements and results. The reviewers showed great interest in the work of the LEDLUM project, raised interesting and qualified questions and provided valuable feedback and recommendations for future project work.

At the end of the day both groups came back together and informed each other

what happened during the day.

At the third and last day of the technical meeting the last two days where quickly reflected and the work plan for the future work in the project has been defined.

Overall, it was a very successful and fruitful meeting and the consortium is looking forward to the upcoming months of the project.



# Technical Progress of the last months

## WP1 "System Architecture"

In WP1 it was further worked on the System Architecture and Requirements (SAnR).

The goal of the SAnR is to integrate the market pull and the technology push of all LEDLUM consortium members to develop a technology that can be the basis of a commercially successful LED driver. The process in which the SAnR of LEDLUM is developed is divided

into several phases to accompany the project through its different stages from concept phase to demonstration.

It is expected that the architecture and requirements will continue to see some adaptations during that phases. All these change requests will be collected and integrated into the next releases of the SAnR.

## WP2 "Passives"

A literature review which surveyed the use of laminated magnetic cores to limit eddy current losses has been done. This survey showed, that laminated magnetic cores are a useful approach to limit eddy current losses. The use of laminations can also prevent the emergence of perpendicular anisotropy which is often a function of magnetic film thickness and contributes further to large material losses at high frequencies. However there is a need to optimize the thickness of insulating interlayer material and the magnetic films to give good performance at high frequencies. The quality of insulating lamination material and seed layer have a significant impact on the coercivity and uniaxial anisotropy of multilayered magnetic films.

A stripline coupled inductor was first designed and fabricated as a test vehicle to develop the CZTB magnetics process flow. The dimensions of device features in the fabricated test vehicles were measured to be within a tolerable limit. The fabricated coupled inductors were characterized for different performance metrics, and the measured data exhibits a rea-

sonable correlation to the FEM simulation results. Therefore, the process integration of the laminated CZTB magnetic stack is validated.

However, a solenoidal magnetic device is deemed more advantageous in the context of process complexity, fabrication cost, current carrying capability and commercial potential. Therefore, integrated solenoidal micro-transformers have been designed for the gate driver application according to the specifications provided by DTU.

Three design variations of the gate driver transformer were developed, all of which satisfy the specified performance metrics. Finally, a brief outline of the solenoid fabrication process using laminated CZTB magnetic stack has been provided.

The first generation integrated solenoidal micro-transformers will be fabricated and characterized in the TNIUCC micro-fabrication and characterization facility. The feedback on the performance of the fabricated devices obtained from the characterization results will be used to further optimize the design of the 2nd generation devices, CZTB magnetic stack and fabrication processes.

## **WP3/4 “Semiconductors” and “Power Electronics”**

The measurement-results of DC/DC closed-loop investigation with focus on interaction between control-circuit and power-semiconductors have been discussed, the requirements and real behavior have been compared and the impact of tolerances and parasitic has been evaluated.

SIP implementing a half-bridge circuitry for an AC-DC and a DC-DC converter have been assembled. The assemblies are comprising a PICS interposer optionally embedding a capacitor into the substrate and a set of external components embedded onto the interposer. The SIP intra-connection is implemented using a combination of soldering, conductive epoxy attachment and wire bonding.

3 configurations of SIP have been delivered. The PICS interposer has been design according DTU/NPC specification in term of parasitic and the embedded capacitor technology

has been proven to withstand the expected peak working voltage with an expected TDDB of 10 years.

Several improvement opportunities have been identified to be implemented for the development of the next demonstrator. They are mainly related to the metallization of the pads of the external components that are not compatible with industrial interconnection process.

The functional characterization of the SIP has started at DTU and NPC. In parallel, detailed electrical characterization of the embedded capacitance is ongoing. This is an important point as long as the trench structure/capacitive electrodes have been optimized for high voltage implementation, and no pre-existing model is available for this specific implementation.

## **WP5 “Driver System”**

The main focus in WP5 in the past months have been to reach MS5 and make delivery D5.1, the first complete LED prototype. This require the work and the results from the previous work package 1-4 to be combined.

### **The work have been carried out in 3 steps:**

**1.** Combine existing building blocks developed in the previous work packages. This resulted in a full system mockup and verified that interfaces between the blocks are working according to the specified system architecture (from WP1).

**2.** Integrate the building blocks on a single PCB to make a platform suitable for further development.

**3.** The last phase was the first attempt to reduce the size and volume of the full system prototype. To limit the overall size of the prototype all the building blocks will were re-structured and placed on the same PCB. The compact platform serves as a demonstrator in combination with luminaries.



## Past Events

### *PCIM - Power Conversion and Intelligent Motion*

5<sup>th</sup> – 7<sup>th</sup> June 2018  
@Nürnberg, Germany

### *Guangzhou International Lighting Exhibition*

9<sup>th</sup> – 12<sup>th</sup> June 2018  
@Guangzhou, China

### *IEEE NANO 2018*

23<sup>rd</sup> – 26<sup>th</sup> July 2018  
@Cork, Ireland

### *LpS 2018 - 8<sup>th</sup> International LED professional Symposium and Expo*

25<sup>th</sup> – 27<sup>th</sup> September 2018  
@Bregenz, Austria

### *PWRSoC2018 - International Workshop on Power Supply on Chip*

17<sup>th</sup> – 19<sup>th</sup> October 2018  
@Hsinchu, Taiwan



## Upcoming Events

### *LUX Live UK*

14<sup>th</sup> – 15<sup>th</sup> November 2018  
@London, UK

### *ISSCC2019 - International Solid-State Circuits Conference*

17<sup>th</sup> – 21<sup>st</sup> February 2019  
@San Francisco (CA), USA

### *APEC2019 - Applied Power Electronics Conference*

17<sup>th</sup> – 21<sup>st</sup> March 2019  
@Anaheim (CA), USA

## Project Partners

